CleverACE Design Guide V1.04

CleverLogic,.Co.Ltd.

Table of Contents

1. Version History

Version	Date	Corrections
V0.90	2012.04.20	작성중
V0.91	2012.04.23	Configuration Data Pin Connection Guide 추가 Ordering Information 추가
V0.92	2012.04.27	CCLK Frequency 추가 Connector 사양 변경
V1.00	2012.07.02	배포
V1.01	2013.01.16	부품 높이 사양 추가
V1.02	2015.11.02	CleverACE2 사양 추가
V1.03	2016.01.04	Mode Select Pin 설정 변경
V1.04	2016.06.07	Bottom View 표기 정정

2. Overview

CleverACE는 FPGA Configuration을 쉽고 빠르게 사용할수 있도록 도와주는 솔루션입니다. 따라서 현 보드를 사용하면 FPGA Configuration을 위한 PROM을 구성하지 않으셔도 됩니다. Xilinx 및 Altera FPGA를 모두 지원하며 대용량 FPGA를 사용할 때 용이합니다.

본 문서는 하드웨어 설계시 고려해야 할 사항에 대하여 정리한 문서입니다.

3. Pin Assignments

- CleverACE assignments
- J2 Connector 1.27mm Pin Header Straight or Hirose DF12-60DS-0.5V (Receptacle) Type
- CCLK Frequency : 96MHz

Number	Pin Name	In/Out/Z	Number	Pin Name	In/Out/ Z
2	+3.3V	VDD	1	+3.3V	VDD
4	+3.3V	VDD	3	+3.3V	VDD
6	GND	VSS	5	GND	VSS
8	Reference Voltage	VREF_IO	7	Reference Voltage	VREF_IO
10	GND	VSS	9	GND	VSS
12	CONF0_PROG	Output/Z	11	CONF0_DONE	Input/Z
14	CONF0_CCLK	Output/Z	13	CONF0_DATA0	Output/Z
16	CONF0_DATA1	Output/Z	15	CONF0_DATA2	Output/Z
18	CONF0_DATA3	Output/Z	17	CONF0_DATA4	Output/Z
20	CONF0_DATA5	Output/Z	19	CONF0_DATA6	Output/Z
22	CONF0_DATA7	Output/Z	21	GND	VSS
24	GND	VSS	23	CONF1_PROG	Output/Z
26	CONF1_DONE	Input/Z	25	CONF1_CCLK	Output/Z
28	CONF1_DATA0	Output/Z	27	CONF1_DATA1	Output/Z
30	CONF1_DATA2	Output/Z	29	CONF1_DATA3	Output/Z
32	CONF1_DATA4	Output/Z	31	CONF1_DATA5	Output/Z
34	CONF1_DATA6	Output/Z	33	CONF1_DATA7	Output/Z
36	GND	VSS	35	GND	VSS
38	CONF2_PROG	Output/Z	37	CONF2_DONE	Input/Z
40	CONF2_CCLK	Output/Z	39	CONF2_DATA0	Output/Z
42	CONF2_DATA1	Output/Z	41	CONF2_DATA2	Output/Z
44	CONF2_DATA3	Output/Z	43	CONF2_DATA4	Output/Z
46	CONF2_DATA5	Output/Z	45	CONF2_DATA6	Output/Z
48	CONF2_DATA7	Output/Z	47	GND	VSS
50	GND	VSS	49	CONF3_PROG	Output/Z
52	CONF3_DONE	Input/Z	51	CONF3_CCLK	Output/Z
54	CONF3_DATA0	Output/Z	53	CONF3_DATA1	Output/Z
56	CONF3_DATA2	Output/Z	55	CONF3_DATA3	Output/Z
58	CONF3_DATA4	Output/Z	57	CONF3_DATA5	Output/Z
60	CONF3_DATA6	Output/Z	59	CONF3_DATA7	Output/Z

- CleverACE2 assignments
- J1 Panasonic AXK6S00547YG 0.5mm pitch
- CCLK Frequency : 96MHz

Number	Pin Name	In/Out/Z	Number	Pin Name	In/Out/ Z
2	+3.3V	VDD	1	+3.3V	VDD
4	+3.3V	VDD	3	+3.3V	VDD
6	GND	VSS	5	GND	VSS
8	Reference Voltage	VREF_IO	7	Reference Voltage	VREF_IO
10	GND	VSS	9	GND	VSS
12	CONF0_PRGB	Output/Z	11	CONF0_DONE	Input/Z
14	CONF0_CCLK	Output/Z	13	CONF0_DATA0	Output/Z
16	CONF0_DATA1	Output/Z	15	CONF0_DATA2	Output/Z
18	CONF0_DATA3	Output/Z	17	CONF0_DATA4	Output/Z
20	CONF0_DATA5	Output/Z	19	CONF0_DATA6	Output/Z
22	CONF0_DATA7	Output/Z	21	CONF1_PRGB	Output/Z
24	CONF1_DONE	Input/Z	23	CONF1_CCLK	Output/Z
26	CONF1_DATA0	Output/Z	25	CONF1_DATA1	Output/Z
28	CONF1_DATA2	Output/Z	27	CONF1_DATA3	Output/Z
30	CONF1_DATA4	Output/Z	29	CONF1_DATA5	Output/Z
32	CONF1_DATA6	Output/Z	31	CONF1_DATA7	Output/Z
34	CONF2_PRGB	Output/Z	33	CONF2_DONE	Input/Z
36	CONF2_CCLK	Output/Z	35	CONF2_DATA0	Output/Z
38	CONF2_DATA1	Output/Z	37	CONF2_DATA2	Output/Z
40	CONF2_DATA3	Output/Z	39	CONF2_DATA4	Output/Z
42	CONF2_DATA5	Output/Z	41	CONF2_DATA6	Output/Z
44	CONF2_DATA7	Output/Z	43	CONF3_PRGB	Output/Z
46	CONF3_DONE	Input/Z	45	CONF3_CCLK	Output/Z
48	CONF3_DATA0	Output/Z	47	CONF3_DATA1	Output/Z
50	CONF3_DATA2	Output/Z	49	CONF3_DATA3	Output/Z
52	CONF3_DATA4	Output/Z	51	CONF3_DATA5	Output/Z
54	CONF3_DATA6	Output/Z	53	CONF3_DATA7	Output/Z
56	GND	VSS	55	GND	
58	CONF4_PRGB	Output/Z	57	CONF4_DONE	Input/Z
60	CONF4_CCLK	Output/Z	59	CONF4_DATA0	Output/Z
62	CONF4_DATA1	Output/Z	61	CONF4_DATA2	Output/Z
64	CONF4_DATA3	Output/Z	63	CONF4_DATA4	Output/Z
66	CONF4_DATA5	Output/Z	65	CONF4_DATA6	Output/Z
68	CONF4_DATA7	Output/Z	67	CONF5_PRGB	Output/Z
70	CONF5_DONE	Input/Z	69	CONF5_CCLK	Output/Z
72	CONF5_DATA0	Output/Z	71	CONF5_DATA1	Output/Z
74	CONF5_DATA2	Output/Z	73	CONF5_DATA3	Output/Z
76	CONF5_DATA4	Output/Z	75	CONF5_DATA5	Output/Z

78	CONF5_DATA6	Output/Z	77	CONF5_DATA7	Output/Z
80	CONF6_PRGB	Output/Z	79	CONF6_DONE	Input/Z
82	CONF6_CCLK	Output/Z	81	CONF6_DATA0	Output/Z
84	CONF6_DATA1	Output/Z	83	CONF6_DATA2	Output/Z
86	CONF6_DATA3	Output/Z	85	CONF6_DATA4	Output/Z
88	CONF6_DATA5	Output/Z	87	CONF6_DATA6	Output/Z
90	CONF6_DATA7	Output/Z	89	CONF7_PRGB	Output/Z
92	CONF7_DONE	Input/Z	91	CONF7_CCLK	Output/Z
94	CONF7_DATA0	Output/Z	93	CONF7_DATA1	Output/Z
96	CONF7_DATA2	Output/Z	95	CONF7_DATA3	Output/Z
98	CONF7_DATA4	Output/Z	97	CONF7_DATA5	Output/Z
100	CONF7_DATA6	Output/Z	99	CONF7_DATA7	Output/Z

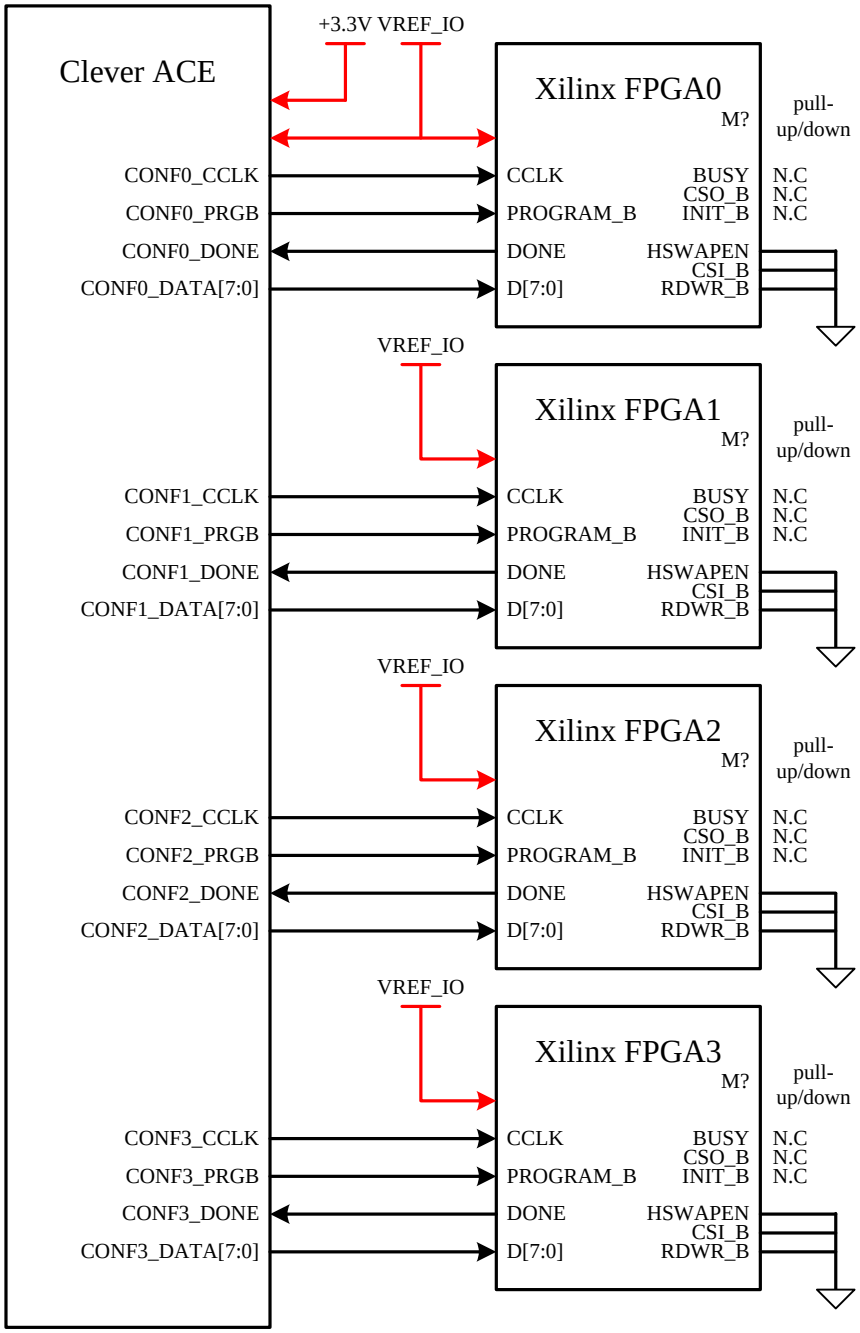
4. FPGA Connection Design

4.1 Xilinx Guide

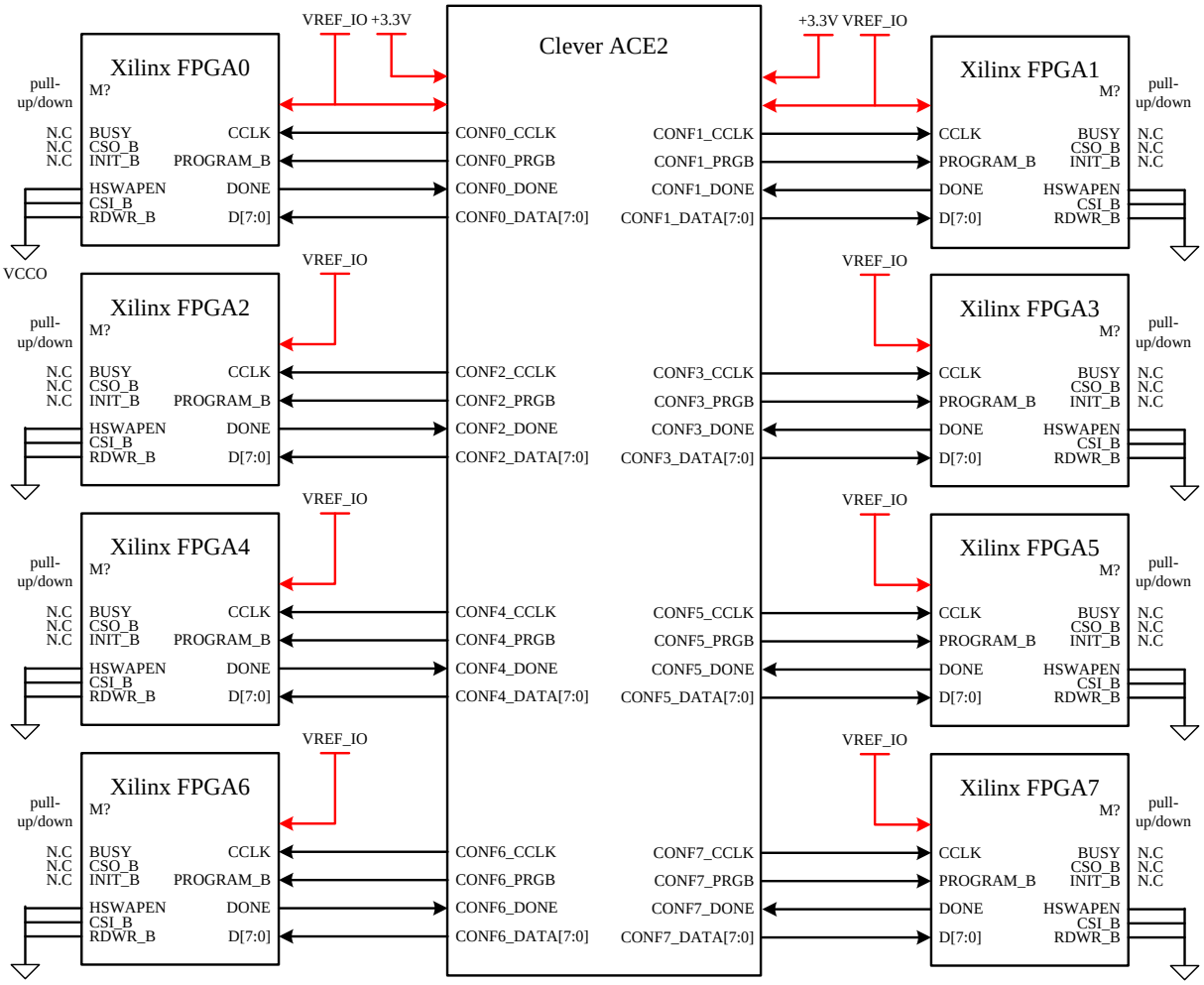
※ CCLK, PROG_B, DONE, DATA[7:0] 핀의 전압을 CleverACE 의 VREF_IO핀에 공급합니다.

※ CCLK, PROG_B, DONE, DATA[7:0] 핀은 CleverACE의 각 핀에 Direct로 연결합니다.

※ Xilinx Slave SelectMAP 설정관련 자세한 사항은 해당 FPGA의 Configuration 메뉴얼을 참고하시기 바랍니다.



[figure] CleverACE Xilinx Slave SelectMAP Mode



[figure] CleverACE2 Xilinx Slave SelectMAP Mode

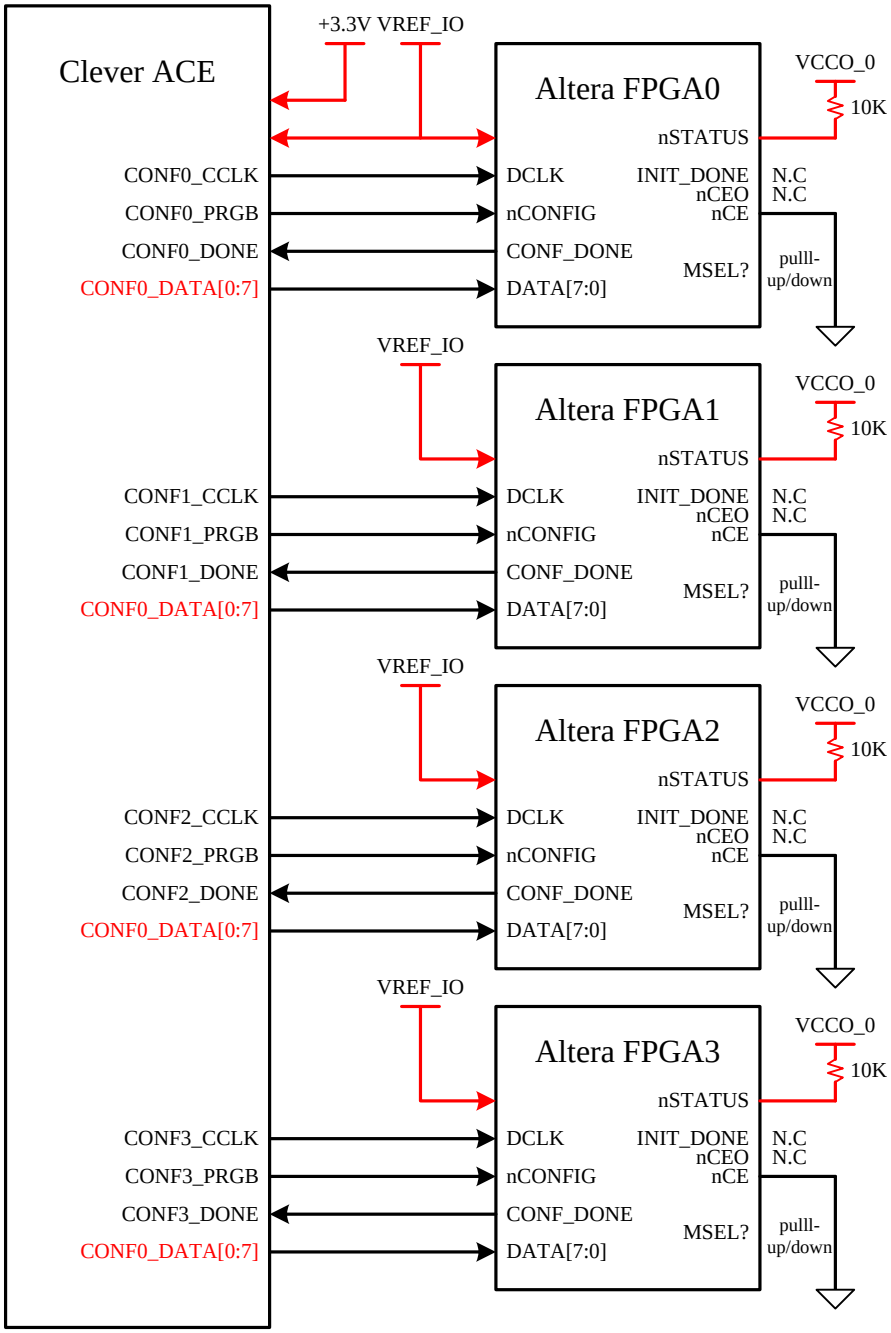
4.2 Altera Guide

※ DCLK, nCONFIG, CONF_DONE, DATA[7:0] 핀의 사용 전압을 CleverACE 의 VREF_IO핀에 공급합니다.

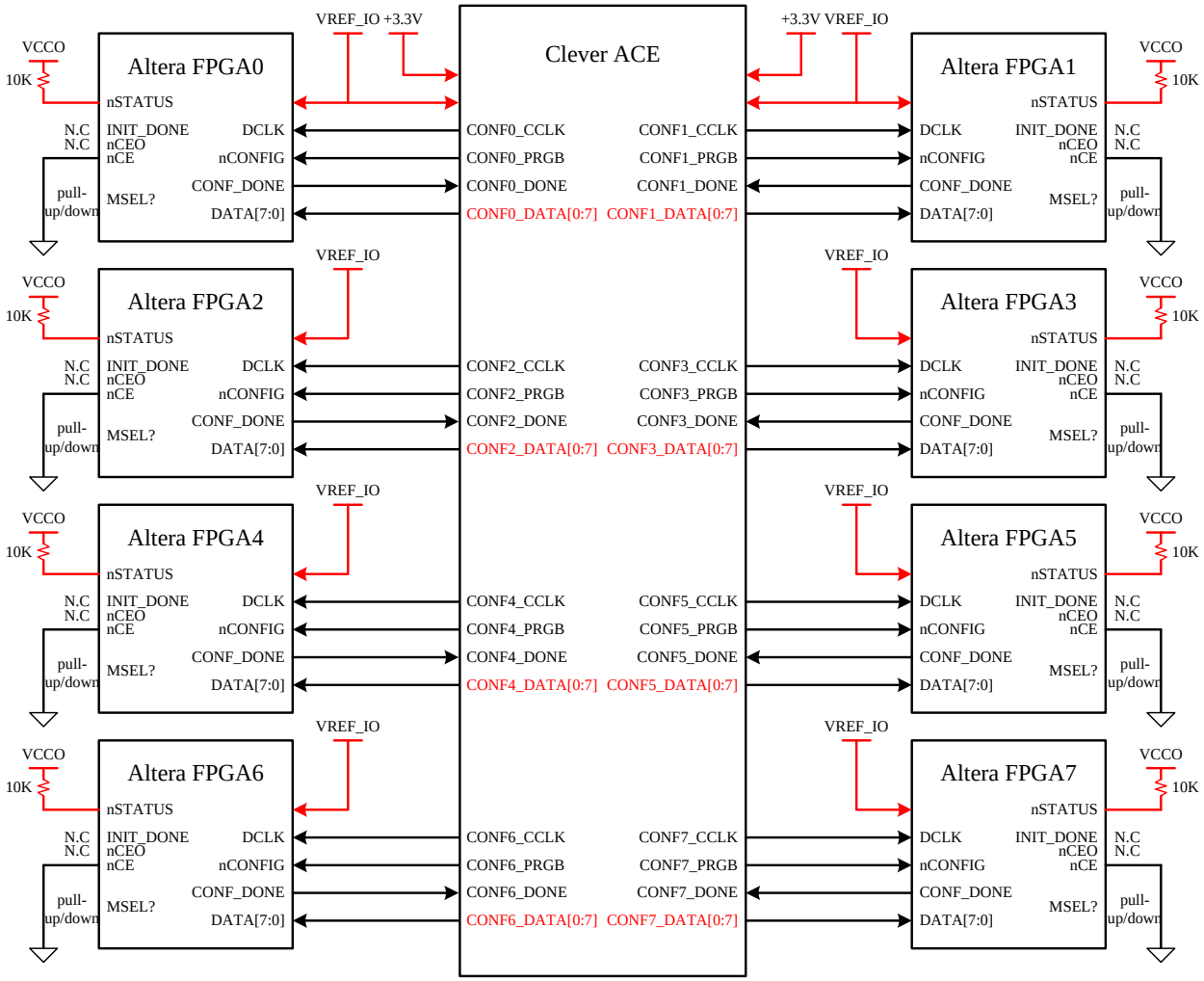
※ DCLK, nCONFIG, CONF_DONE 핀은 CleverACE의 각 핀에 Direct로 연결하고, DATA[7:0]은 Cross로 연결합니다.

※ INIT_DONE핀은 N.C처리 하셔도 됩니다.

※ Altera FPP Mode 설정관련 자세한 사항은 해당 FPGA의 Configuration 메뉴얼을 참고하시기 바랍니다.



[figure] CleverACE Altera Fast Passive Parallel (FPP) Mode

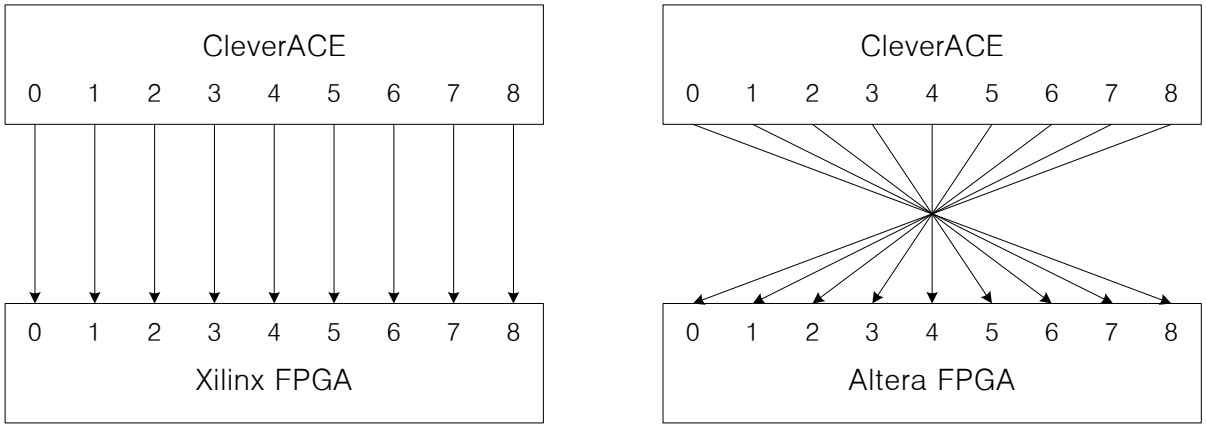


[figure] CleverACE2 Altera Fast Passive Parallel (FPP) Mode

4.3 Configuration Data Connection Guide

※ Data Pin 연결시 주의 하여야 합니다.

※ 아래와 같이 Xilinx는 Direct로 연결하고 Altera는 Cross로 연결합니다.



5. Ordering Information

EX) C L A - 1 0 0 A

A: 1.27mm Pin Header Straight Type
B: Hirose DF12-60DS-0.5V (Receptacle)
C: Panasonic AXK6S00547YG (Header)

Revision History
- 100, 200, ...

CleverLogic's Advanced Configuration Environment

Part Number	Connector Type	Operational Range
CLA-100A	1.27mm Pin Header Straight Type	Commercial (0℃ to 85℃)
CLA-100B	Hirose DF12-60DS-0.5V (Receptacle)	
CLA-200C	Panasonic AXK6S00547YG (Header)	

6. Electrical Specifications

6.1 Absolute Maximum Ratings

-VCC : 0.5V to +3.75V

-VREF_IO : 0.5V to +3.75V

6.2 Operating Ranges

6.2.1 Temperature Ranges

◦ Commercial Temperature 0℃ to +85℃

6.2.2 Power Supply Voltages

-VCC : 3.3V

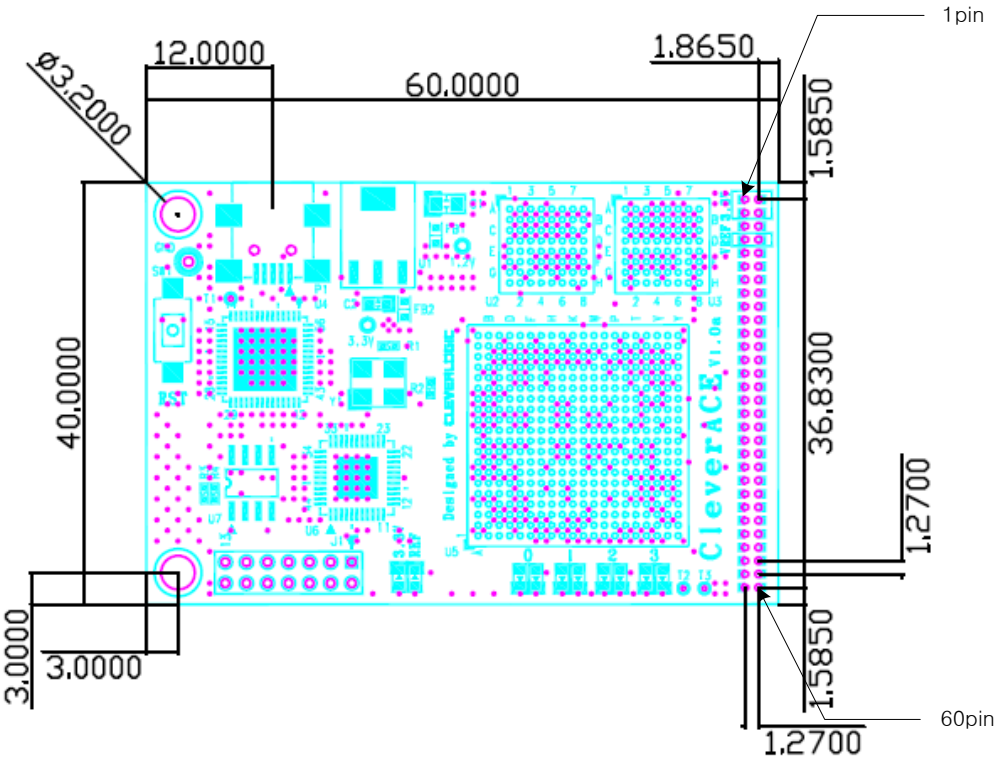
-VREF_IO : 1.8V or 2.5V or 3.3V

-Current : 3.3V / 500mA / 1.65W

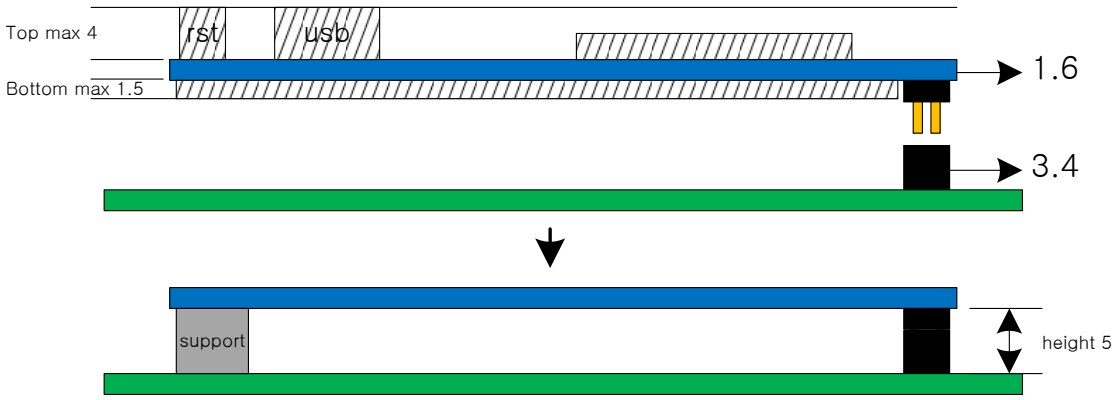
7. Outline Dimensions

- Unit of Measure = mm

7.1 A Type

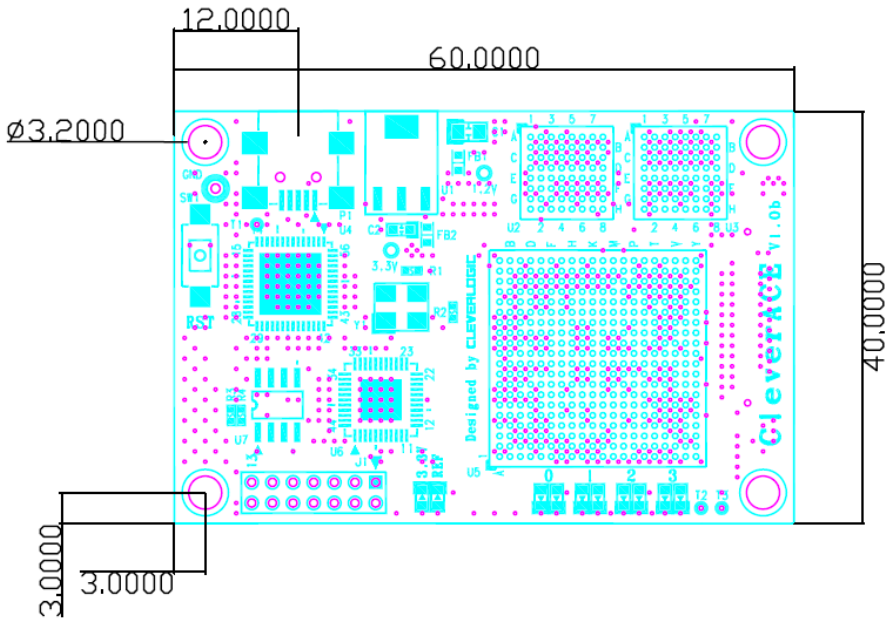


A Type Connector TOP_VIEW

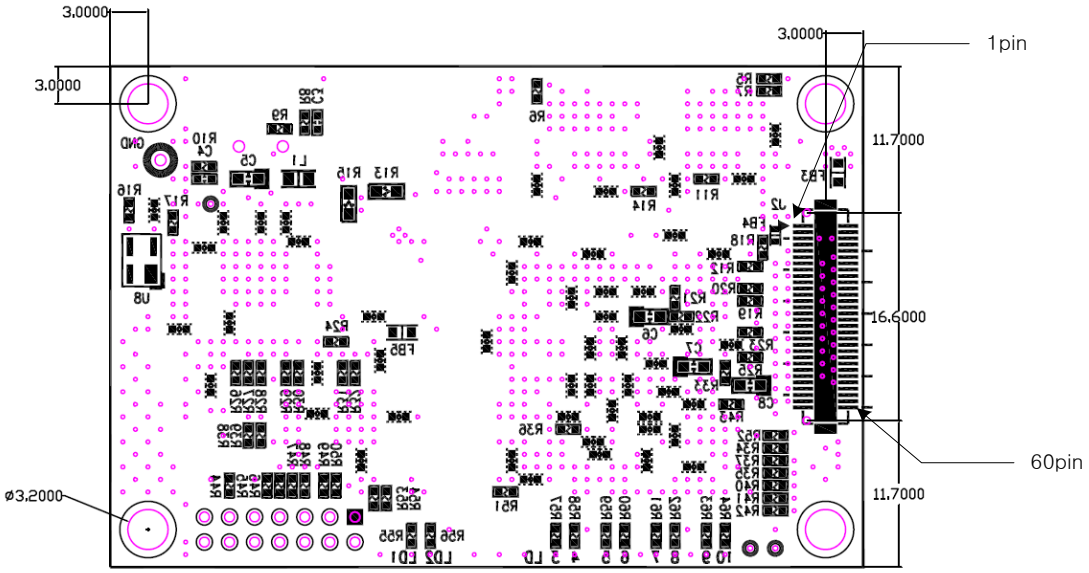


A Type Parts height

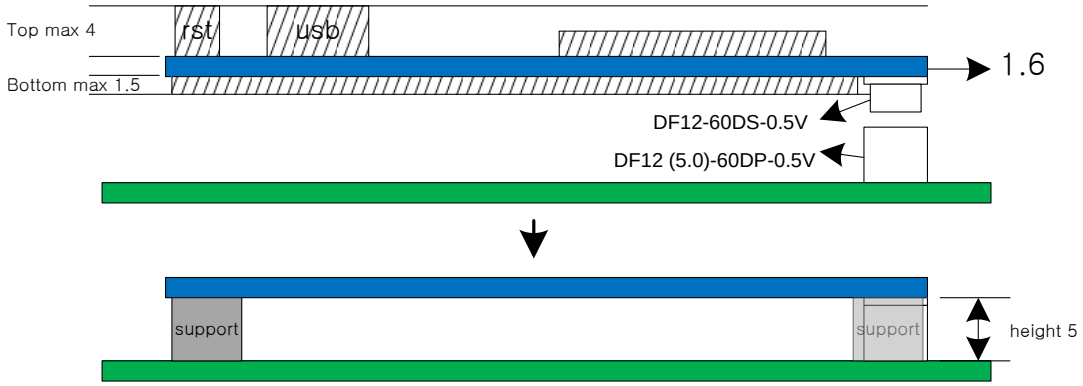
7.2 B Type



B Type Connector TOP_VIEW

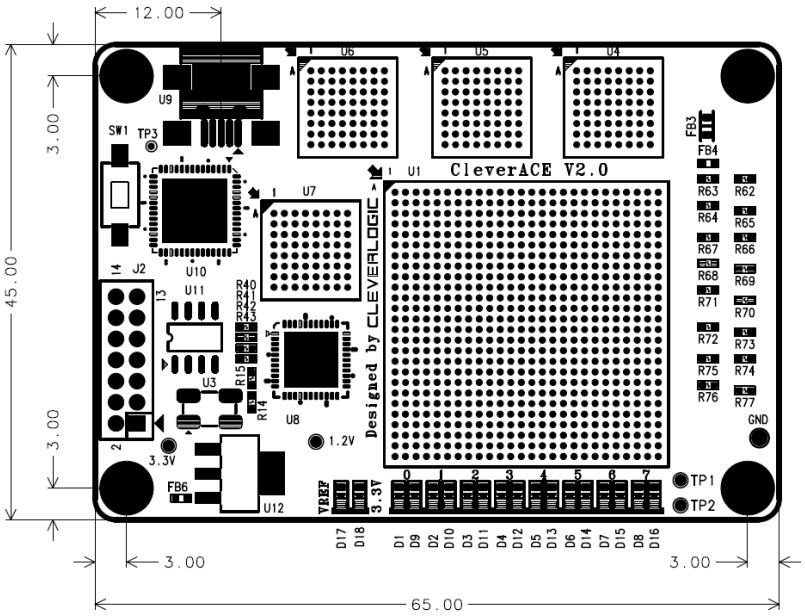


B Type Connector Perspective VIEW

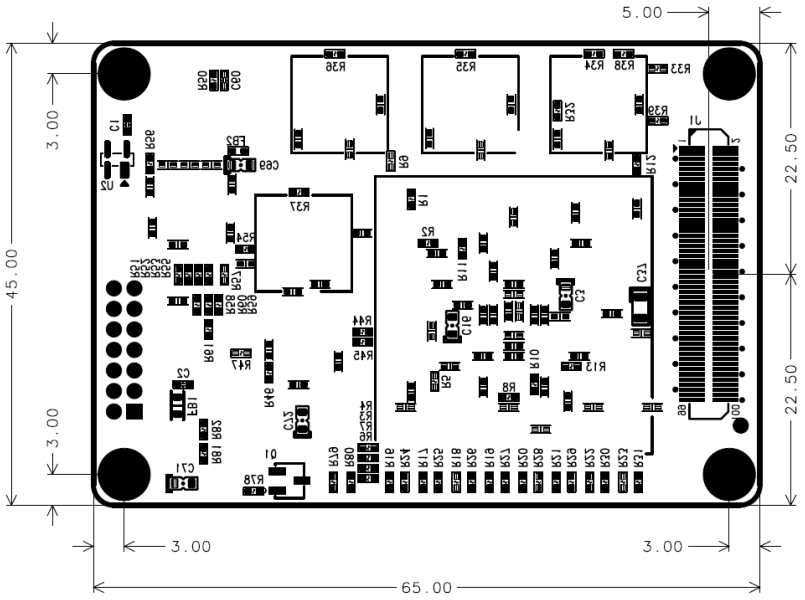


B Type Parts height

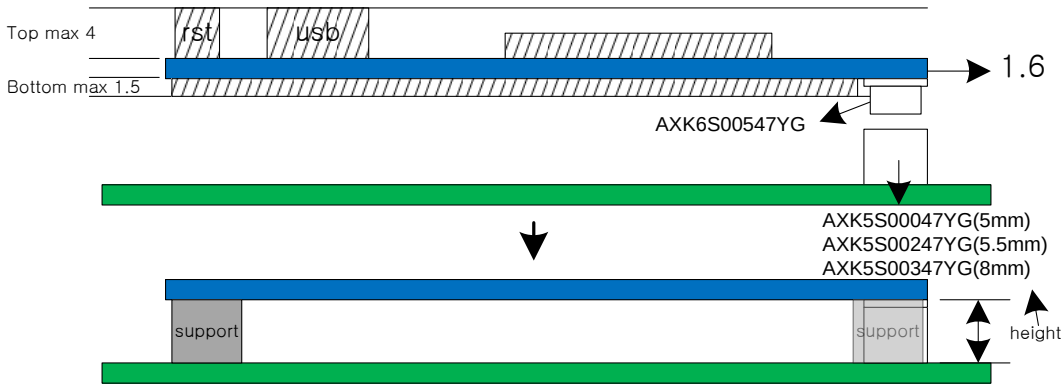
7.3 C Type



B Type Connector TOP VIEW



B Type Connector Perspective VIEW



C Type Parts height