CleverACE Design Guide V1.01

CleverLogic,.Co.Ltd.

Table of Contents

1. Version History

Version	Date	Corrections
V0.90	2012.04.20	작성중
V0.91	2012.04.23	Configuration Data Pin Connection Guide 추가 Ordering Information 추가
V0.92	2012.04.27	CCLK Frequency 추가 Connector 사양 변경
V1.00	2012.07.02	배포
V1.01	2013.01.16	부품 높이 사양 추가

2. Overview

CleverACE는 FPGA Configuration을 쉽고 빠르게 사용할수 있도록 도와주는 솔루션입니다. 따라서 현 보드를 사용하면 FPGA Configuration을 위한 PROM을 구성하지 않으셔도 됩니다. Xilinx 및 Altera FPGA를 모두 지원하며 대용량 FPGA을 사용할 때 용이합니다.

본 문서는 하드웨어 설계시 고려해야 할 사항에 대하여 정리한 문서입니다.

3. Pin Assignments

- J2 Connector 1.27mm Pin Header Straight or Hirose DF12-60DS-0.5V (Receptacle) Type
- CCLK Frequency : 96MHz

Number	Pin Name	In/Out/Z	Number	Pin Name	In/Out/ Z
2	+3.3V	VDD	1	+3.3V	VDD
4	+3.3V	VDD	3	+3.3V	VDD
6	GND	VSS	5	GND	VSS
8	Reference Voltage	VREF_IO	7	Reference Voltage	VREF_IO
10	GND	VSS	9	GND	VSS
12	CONF0_PROG	Output/Z	11	CONF0_DONE	Input/Z
14	CONF0_CCLK	Output/Z	13	CONF0_DATA0	Output/Z
16	CONF0_DATA1	Output/Z	15	CONF0_DATA2	Output/Z
18	CONF0_DATA3	Output/Z	17	CONF0_DATA4	Output/Z
20	CONF0_DATA5	Output/Z	19	CONF0_DATA6	Output/Z
22	CONF0_DATA7	Output/Z	21	GND	VSS
24	GND	VSS	23	CONF1_PROG	Output/Z
26	CONF1_DONE	Input/Z	25	CONF1_CCLK	Output/Z
28	CONF1_DATA0	Output/Z	27	CONF1_DATA1	Output/Z
30	CONF1_DATA2	Output/Z	29	CONF1_DATA3	Output/Z
32	CONF1_DATA4	Output/Z	31	CONF1_DATA5	Output/Z
34	CONF1_DATA6	Output/Z	33	CONF1_DATA7	Output/Z
36	GND	VSS	35	GND	VSS
38	CONF2_PROG	Output/Z	37	CONF2_DONE	Input/Z
40	CONF2_CCLK	Output/Z	39	CONF2_DATA0	Output/Z
42	CONF2_DATA1	Output/Z	41	CONF2_DATA2	Output/Z
44	CONF2_DATA3	Output/Z	43	CONF2_DATA4	Output/Z
46	CONF2_DATA5	Output/Z	45	CONF2_DATA6	Output/Z
48	CONF2_DATA7	Output/Z	47	GND	VSS
50	GND	VSS	49	CONF3_PROG	Output/Z
52	CONF3_DONE	Input/Z	51	CONF3_CCLK	Output/Z
54	CONF3_DATA0	Output/Z	53	CONF3_DATA1	Output/Z
56	CONF3_DATA2	Output/Z	55	CONF3_DATA3	Output/Z
58	CONF3_DATA4	Output/Z	57	CONF3_DATA5	Output/Z
60	CONF3_DATA6	Output/Z	59	CONF3_DATA7	Output/Z

4. FPGA Connection Design

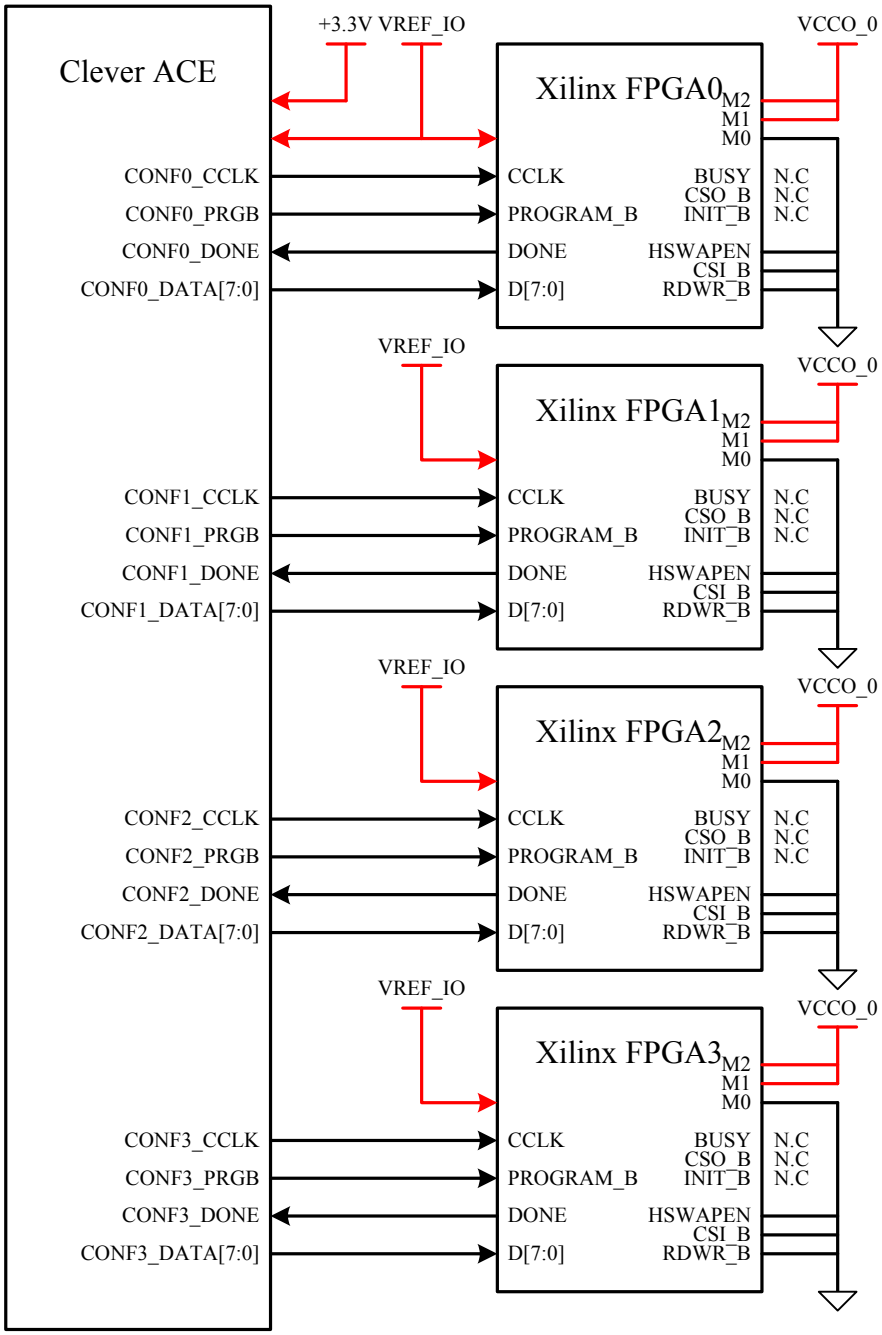
4.1 Xilinx Guide

※ CCLK, PROG_B, DONE, DATA[7:0] 핀의 전압을 CleverACE 의 VREF_IO핀에 공급합니다.

※ CCLK, PROG_B, DONE, DATA[7:0] 핀은 CleverACE의 각 핀에 Direct로 연결합니다.

※ Xilinx의 Mode는 M[2:0] : 110으로 설정합니다.

※ CSI_B와 RDWR_B 핀은 GND에 연결합니다.



[figure] Xilinx Slave SelectMAP Mode

4.2 Altera Guide

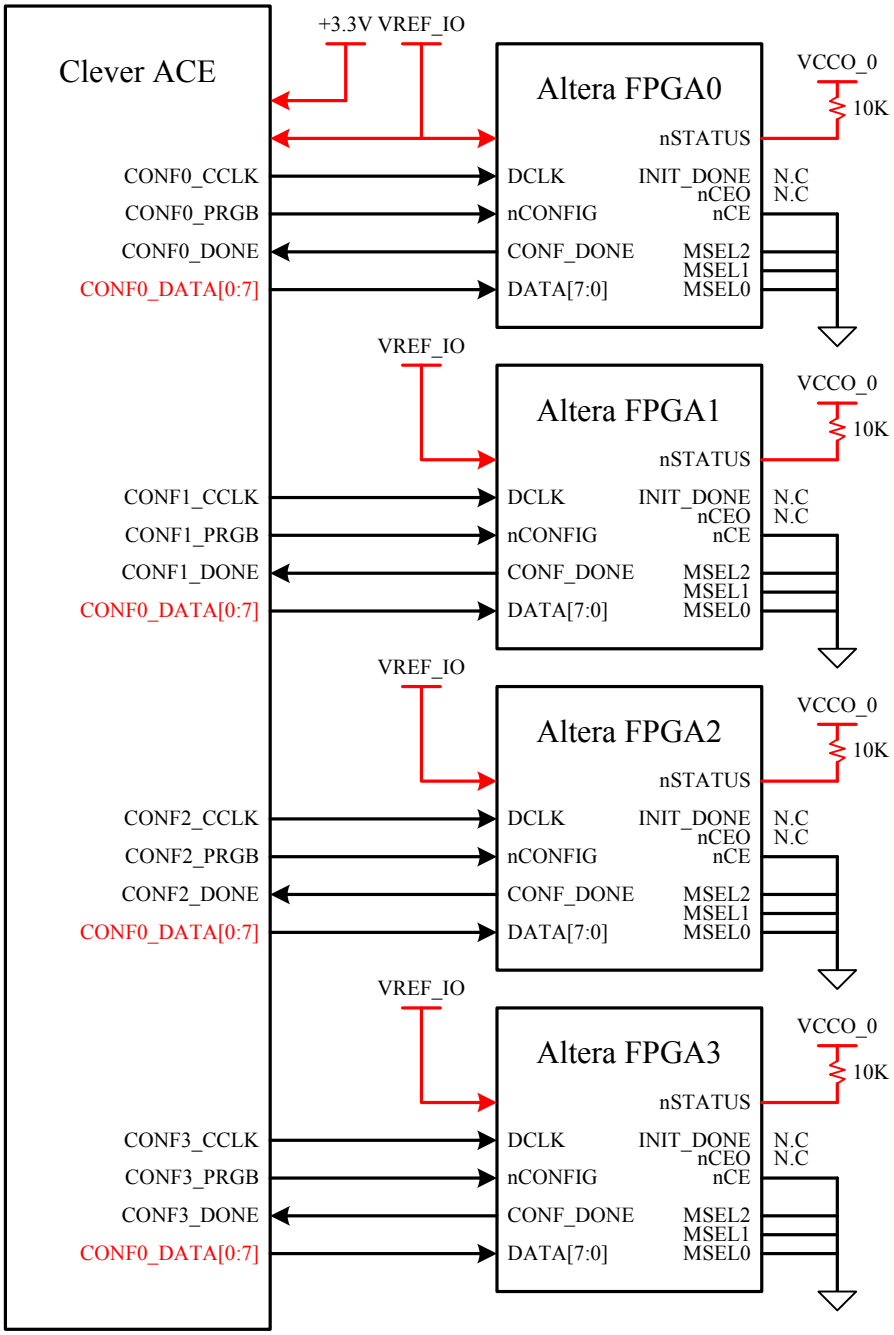
※ DCLK, nCONFIG, CONF_DONE, DATA[7:0] 핀의 사용 전압을 CleverACE 의 VREF_IO핀에 공급합니다.

※ DCLK, nCONFIG, CONF_DONE 핀은 CleverACE의 각 핀에 Direct로 연결하고, DATA[7:0]은 Cross로 연결합니다.

※ Configuration Mode는 FPP Mode로 설정합니다. MSEL[2:0] : 000

※ nSTATUS는 Pull-up 10K 저항으로 연결합니다.

※ INIT_DONE핀은 N.C처리 하셔도 됩니다.

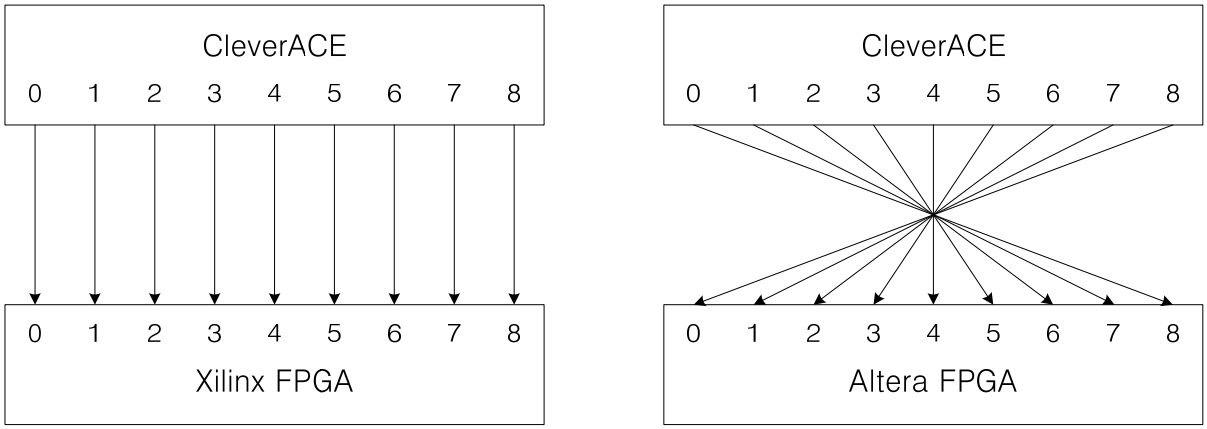


[figure] Altera Fast Passive Parallel (FPP) Mode

4.3 Configuration Data Connection Guide

※ Data Pin 연결시 주의 하여야 합니다.

※ 아래와 같이 Xilinx는 Direct로 연결하고 Altera는 Cross로 연결합니다.



5. Ordering Information

EX) C L A - 1 0 0 A

A: 1.27mm Pin Header Straight Type
B: Hirose DF12-60DS-0.5V (Receptacle)

Revision History
- 100, 200, ...

CleverLogic's Advanced Configuration Environment

Part Number	Connector Type	Operational Range
CLA-100A	1.27mm Pin Header Straight Type	Commercial (0℃ to 85℃)
CLA-100B	Hirose DF12-60DS-0.5V (Receptacle)	

6. Electrical Specifications

6.1 Absolute Maximum Ratings

-VCC : 0.5V to +3.75V

-VREF_IO : 0.5V to +3.75V

6.2 Operating Ranges

6.2.1 Temperature Ranges

- Commercial Temperature 0°C to +85°C

6.2.2 Power Supply Voltages

-VCC : 3.3V

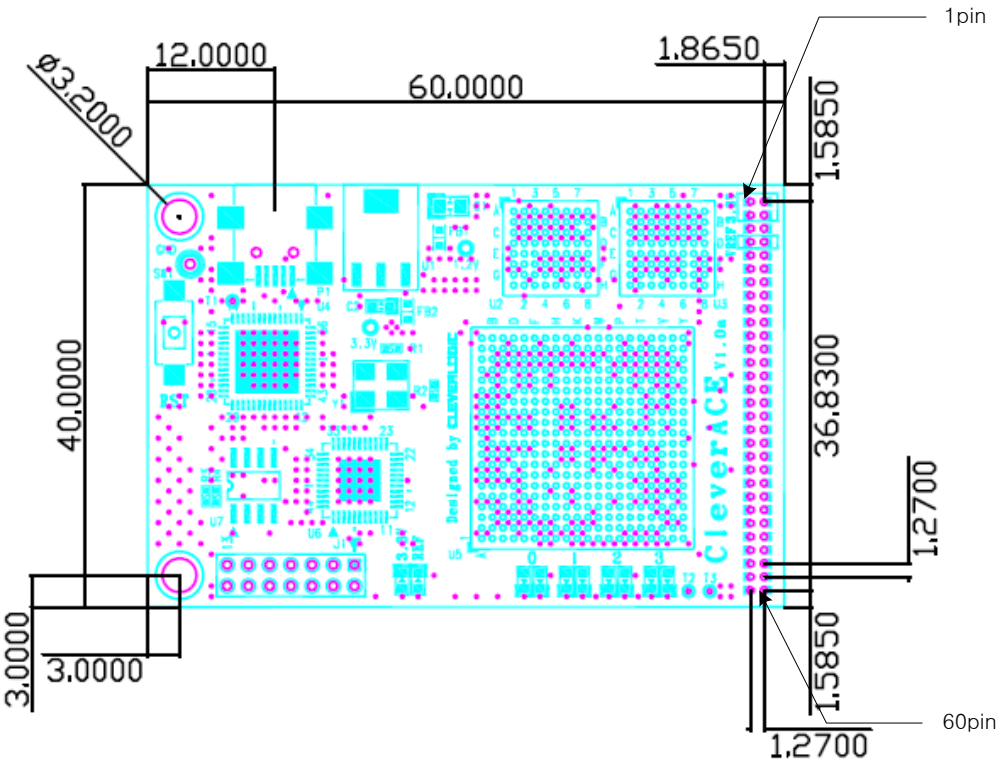
-VREF_IO : 1.8V or 2.5V or 3.3V

-Current : 3.3V / 500mA / 1.65W

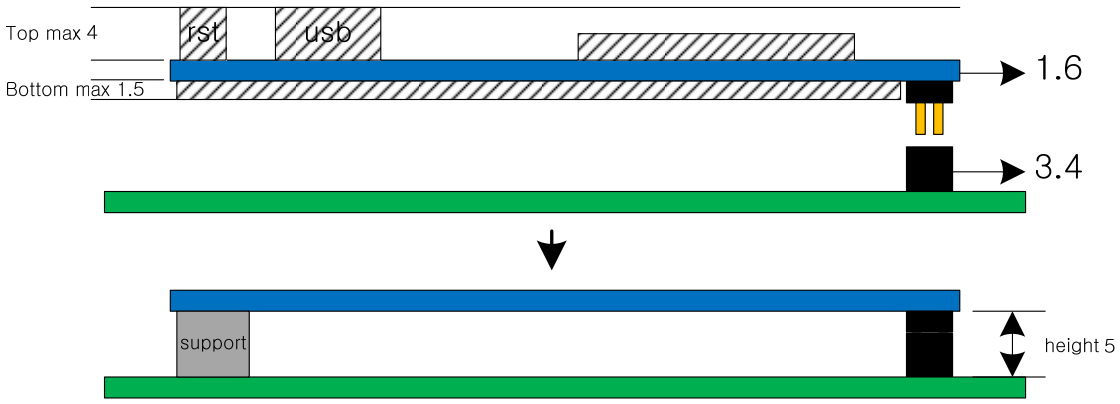
7. Outline Dimensions

- Unit of Measure = mm

7.1 A Type

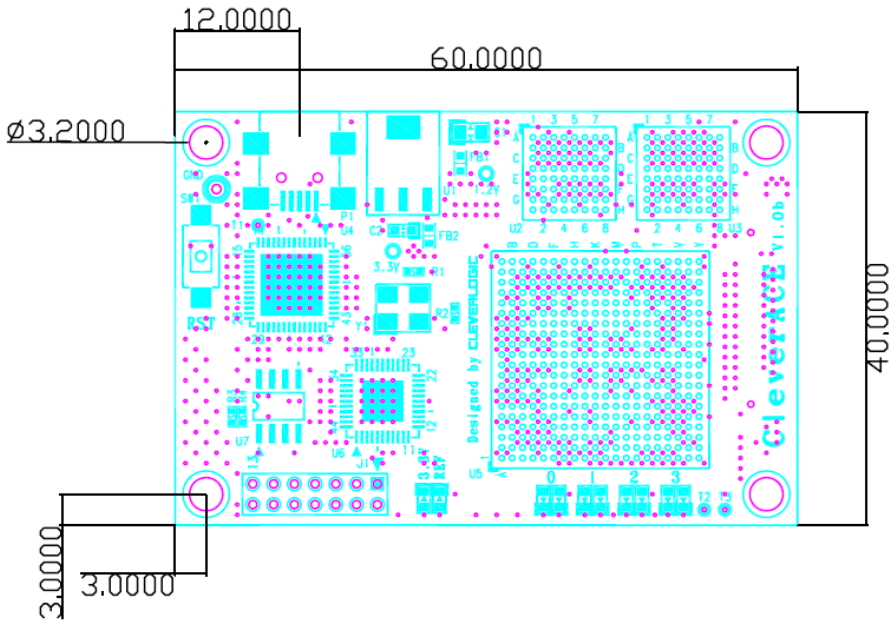


A Type Connector TOP_VIEW

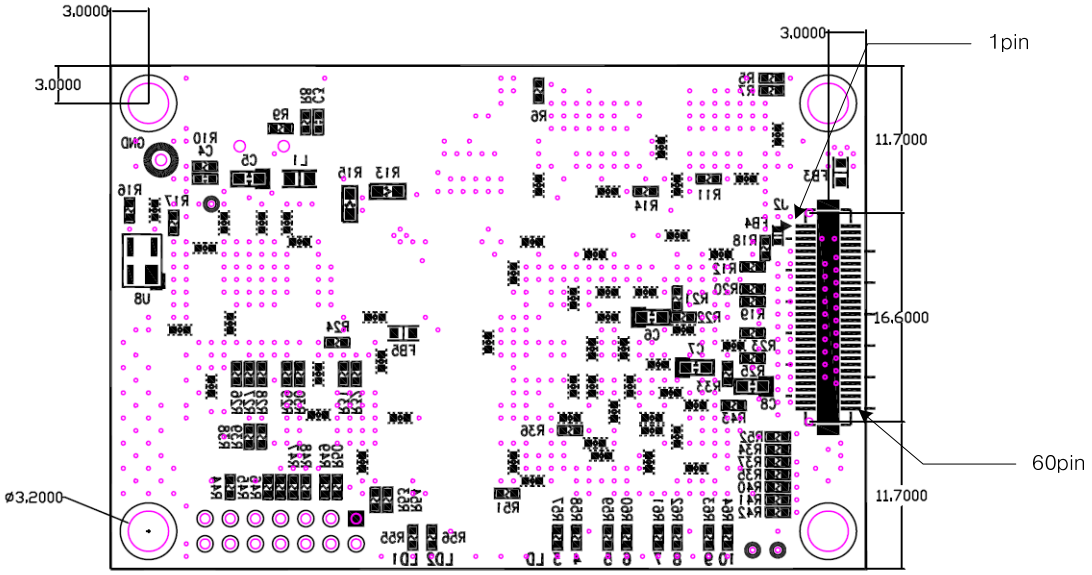


A Type Parts height

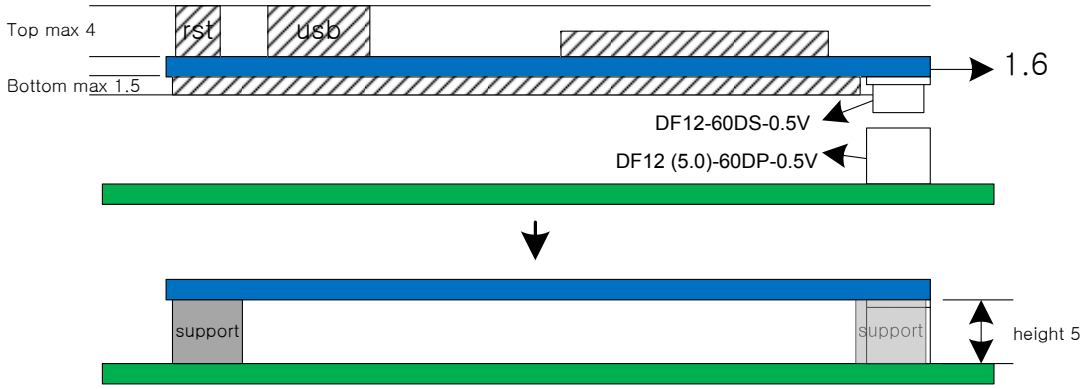
7.2 B Type



B Type Connector TOP_VIEW



B Type Connector BOTTOM_VIEW



B Type Parts height